DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features, a parasitic npn transistor (claim 9), and a thyristor (claim 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: Specification recites a "time delay means" on Page 3, but no explanation of the time delay means is provided on Pages 6-8 of the Specification, to provide information on how the time delay means affect the circuit operation, when specific operation of the circuit/s is discussed. Appropriate correction is required. Applicant should be careful not to introduce any new matter into the disclosure (i.e., matter which is not supported by the disclosure as originally filed).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims1-2, 4-9, 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US 5,617,283) in view of Chin et al. (US 5,430,602). Regarding Claim 1, Krakauer discloses an integrated protection circuit for an integrated circuit device (Figures 1-2), comprising: a first transistor 45a (Figure 2) whose control outputs are connected between a pad 12 and a control input of a clamping device 18, control outputs of said clamping device being connected between said pad and a reference voltage terminal VSS,

a second transistor 45b whose control outputs are connected between the control input of the clamping device and said reference voltage terminal, and

a time-delay circuit including a capacitive device 42 (42 is a diode connected PMOS transistor having a diode capacitance) connected between a supply voltage terminal 16 and said control inputs of said first transistor and said second transistor. Krakauer does not specifically disclose a resistor in series with the capacitive device (Krakauer's delay circuit has the resistive components from the connection means and that from the diode connected transistor).

Chin discloses a protection circuit for an integrated circuit (Figure 2), where a resistor R1, R2' connected in series with a capacitive device T1 (T1 is diode connected MOS transistor) and connected to pad 110. It would be obvious to one of ordinary skill in the art at the time the invention was made to provide a resistor in series with the capacitive device of Krakauer, to protect the MOS transistor by providing current limiting means between the pad and the transistor, and Chin teaches that a resistor connected in series with a diode connected MOS transistor to protect the transistor (Column 3, lines 38-40).

Regarding Claim 2, Krakauer discloses that the pad 12 is a signal pad or a power supply pad (Column 4, lines 3-7).

Regarding Claim 4, Krakauer discloses that the time delay means comprises a third transistor 42, the resistance means (wire resistance) being connected between the supply voltage terminal and said third transistor, said third transistor forming the capacitive device. Krakauer's third transistor is a diode connected PMOS transistor, whereas the claimed element is diode connected NMOS transistor, and the recited node connection differs, and it would be obvious to one of ordinary skill in the art to use an

NMOS or PMOS transistor in a diode connected configuration to use as a capacitive device.

Regarding Claim 5, Krakauer discloses that a fourth transistor 46 provided whose control outputs are connected between the reference voltage terminal and the control output of the third transistor. Krakauer does not disclose that that control input is connected to said reference voltage terminal (Krakauer has a diode connected MOS transistor whereas the claim recites a grounded gate MOS transistor). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a grounded gate MOS transistor, in place of a diode connected MOS transistor, because both connections remain off during normal operation of IC, and are used to clamp voltages during an ESD event, and differs only where the gate is connected to operate as a clamp, and the selection is based on the design requirements.

Regarding Claims 6 and 8, Krakauer discloses that the first transistor (MP1) is a p-channel MOS transistor (45a is a PMOS transistor), and the clamping device is an n-channel MOS transistor laid out for ESD protection (see Figure 2).

Regarding Claim 7, Krakauer discloses that the second and fourth transistors are n-channel MOS transistors. Krakauer does not disclose that the third transistor is n-channel MOS transistor (Krakauer's third transistor is a p-channel MOS transistor). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an n-channel MOS transistor for the third transistor also, because n-channel and p-channel MOS transistors are art recognized equivalents.

Regarding Claim 9, Krakauer discloses the clamping device 18 which forms a parasitic npn transistor (clamping device 18 of Krakauer is an NMOS transistor having inherent feature of forming a parasitic npn transistor between the drain, bulk, and source region of the transistor based on the level of ESD voltage).

Regarding Claim 12, Krakauer discloses an integrated protection circuit for protecting an integrated circuit device, the protection circuit comprising: a clamping device 18 having a control input and two control outputs, the control outputs including a first control output coupled to a pad 12 and a second control output coupled to a reference voltage terminal V_{SS};

a first transistor 45a having control outputs connected between the pad and the control input of the clamping device;

a second transistor 45b having control outputs connected between the reference voltage terminal and the control input of the clamping device; and

a time-delay circuit including a capacitive device 42 connected in series between a power supply 16 and the control inputs of the first and second transistors, the capacitive device being connected to the control inputs of the first and second transistors. Krakauer does not specifically disclose a resistor in series with the capacitive device (Krakauer's delay circuit has the resistive components from the connection means and that from the diode connected transistor).

Chin discloses a protection circuit for an integrated circuit (Figure 2), where a resistor R1, R2' connected in series with a capacitive device T1 (T1 is diode connected MOS transistor) and connected to pad 110. It would be obvious to one of ordinary skill

in the art at the time the invention was made to provide a resistor in series with the capacitive device of Krakauer, to protect the MOS transistor by providing current limiting means between the pad and the transistor, and Chin teaches that a resistor connected in series with a diode connected MOS transistor to protect the transistor (Column 3, lines 38-40).

Regarding Claim 13, Krakauer discloses that the capacitive device is not directly coupled to the pad (capacitive device 42 is connected to PAD 12 through metal line/ connection), Chin discloses that the capacitive device T1 is not directly connected to PAD 110 (T1 is connected to PAD 110 by metal line as well as resistor R1, R2').

Regarding Claim 14, Chin discloses that the resistor is directly connected to the capacitive device with no intervening circuits (see T1 directly connected to R2', R1 in Figure 3).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US 5,617,283) in view of Chin et al. (US 5,430,602) and Ker et al. (US 2002/0050615, Ker '615). Regarding Claim 10, Krakauer does not disclose a thyristor device. Ker '615 discloses an ESD protection circuit (see Figure 7b) comprising a clamping device which is a thyristor (see nSCR device). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Krakauer and Chin, and to use a thyristor in place of the MOS transistor, because Ker '615 teaches the use of thyristor as ESD clamping device for the protection of integrated circuits from ESD and EOS.

6. Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krakauer et al. (US 5,617,283) in view of Chin et al. (US 5,430,602) and Lai et al. (US 2003/0235022). Regarding Claims 11and 15, Krakauer does not disclose a diode between the pad and the supply voltage terminal. Lai discloses an ESD protection circuit comprising a diode 52 connected between a pad 40 and a power supply voltage terminal 50 (see Figure 4A). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Krakauer and Chin, and to provide a diode as taught by Lai to provide and ESD path from PAD to the power supply pad to protect the IC and to isolate the pads during normal operation.

7. Claims 1-2, 4-9, 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over John et al. (US 6,522,511) in view of Ker et al. (US 6,912,109, Ker '109). Regarding Claim 1, John discloses an integrated protection circuit for an integrated circuit device (Figures 1-3), comprising: a first transistor (PMOS of 32 in Figure 3) whose control outputs are connected between a pad 22 and a control input of a clamping device 34, control outputs of said clamping device being connected between said pad and a reference voltage terminal 20,

a second transistor (NMOS of 32) whose control outputs are connected between the control input of the clamping device and said reference voltage terminal, and

a time-delay circuit including a resistor (see resistor of 30) connected between a supply voltage terminal 18 and said control inputs of said first transistor and said second transistor. John does not disclose a capacitive device connected in series with the resistor (wiring connection of John has some capacitance).

Ker '109 discloses an ESD protection circuit for integrated circuit (Figures 1-3, 11-22) comprising a time delay circuit including a capacitive device 42 (Figures 11, 13) and a resistor 44, 46 (Figures 11, 13) and the combination of the capacitive device and the resistor connected in series between the supply voltage terminal VDD and control inputs of a first transistor 28 and a second transistor 30, output of 28, 30 controlling a clamping device 32. Ker also teaches that the resistive element in a delay circuit can be implemented using poly resistor, a diffusion resistor, or a well resistor, as well as using an active NMOS or PMOS device, and that the capacitive element can be implemented by metal capacitor or by MOS gate capacitor (Column 9, lines 48-62). It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit of John and to add a capacitive device in the time delay circuit as taught by Ker '109 to more accurately control the triggering or turning on of the inverter 32, and in turn the triggering or turning on of the clamping device 34 of John, because a MOS transistor connected as a capacitive device acts as a switch also and remains until the threshold voltage is met such that no current flows though the path, and the resistor of John would be protecting the capacitive device added (see Ker '109, Column 9, lines 65-67).

Regarding Claim 2, John discloses that the pad 22 is a signal pad or a power supply pad (see non-external power supply pad 22 recited in Column 3, lines 5-7).

Regarding Claim 4, John discloses the resistor 30, Ker '109 discloses a third transistor 42, the third transistor forming the capacitive device, and that John resistor can be implemented using a MOS transistor or a third transistor (Column 9, lines 48-

62), and would be obvious to implement the capacitive device 42 of Ker as a diode connected transistor to have the resistor end connected to the gate/source connected node of the transistor.

Regarding Claim 5, John discloses a fourth transistor (MOS transistor of 30) provided whose control outputs are connected between a reference voltage terminal 20 and the control output of the third transistor and whose control input is connected to said reference voltage terminal (see connection of elements in 30), and Ker '109 discloses a fourth transistor 34 provided whose control outputs are connected between a reference voltage terminal VSS and the control output of the third transistor and whose control input is connected to said reference voltage terminal (see connection of 42, 34, 36 in Figure 13).

Regarding Claims 6 John and Ker '109 discloses that the first transistor is a p-channel MOS transistor (see John, Figure 3, PMOS of 32; Ker '109, Figure 11, 28 is PMOS and 30 is NMOS).

Regarding Claim 7, John discloses that the second and fourth transistors are n-channel MOS transistors. Ker '109 discloses that the second transistor is NMOS transistor, third is a PMOS transistor, and fourth is an NMOS or PMOS (PMOS 34 Figure 13, NMOS 38 in Figure 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an n-channel MOS transistor or –channel transistor for the second, third, and transistors (that are diode connected transistors for implementing a capacitor or a resistor or MOS capacitor), because n-channel and p-channel MOS transistors are art recognized equivalents.

Regarding Claim 8, John discloses that the clamping device is an n-channel MOS transistor laid out for ESD protection (34 is an NMOS).

Regarding Claim 9, John discloses the clamping device 34 which forms a parasitic npn transistor (clamping device 34 of John is a MOS transistor having inherent feature of forming a parasitic npn, or pnp bipolar transistor depending on an NMOS or PMOS transistor between the drain, bulk, and source region of the transistor based on the level of ESD voltage), and Ker '109 discloses a clamping device which forms a parasitic npn transistor (Figure 21, Column 11, lines 11-31).

Regarding Claim 11, John discloses a diode 44 between the pad and the supply voltage terminal.

Regarding Claim 12, John discloses an integrated protection circuit for protecting an integrated circuit device (Figures 1-3), the protection circuit comprising: a clamping device 34 having a control input and two control outputs , the control outputs including a first control output coupled to a pad 22 and a second control output coupled to a reference voltage terminal 20;

a first transistor (PMOS transistor of inverter 32) having control outputs connected between the pad and the control input of the clamping device;

a second transistor (NMOS transistor of 32) having control outputs connected between the reference voltage terminal and the control input of the clamping device; and

a time-delay circuit including a resistor (resistor element of 30 in Figure 3) connected in series between a power supply 18 and the control inputs of the first and

second transistors, the resistor being connected to the power supply and to the control inputs of the first and second transistors.

John also discloses the metal line connection with capacitance, but does not disclose a capacitive device connected in series with the resistor.

Ker '109 discloses an ESD protection circuit for integrated circuit (Figures 1-3, 11-22) comprising a time delay circuit including a capacitive device 42 (Figures 11, 13) and a resistor 44, 46 (Figures 11, 13) and the combination of the capacitive device and the resistor connected in series between the supply voltage terminal VDD and control inputs of a first transistor 28 and a second transistor 30, output of 28, 30 controlling a clamping device 32. Ker also teaches that the resistive element in a delay circuit can be implemented using poly resistor, a diffusion resistor, or a well resistor, as well as using a active NMOS or PMOS device, and that the capacitive element can be implemented by metal capacitor or by MOS gate capacitor (Column 9, lines 48-62). It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit of John and to add a capacitive device in the time delay circuit as taught by Ker '109 to more accurately control the triggering or turning on of the inverter 32, and in turn the triggering or turning on of the clamping device 34 of John, because a MOS transistor connected as a capacitive device acts as a switch also and remains until the threshold voltage is met such that no current flows though the path, and the resistor of John would be protecting the capacitive device added (see Ker '109, Column 9, lines 65-67).

Regarding Claim 13-14, John discloses that the (metal line) capacitance is not directly coupled to the pad, the resistor is directly connected to the capacitance with no intervening circuits, and Ker discloses that the capacitive device 42 is not directly coupled to the pad (42 is connected to pad metal line/connection means) and the resistor 44, 46 is directly connected to the capacitive device with no intervening circuits.

Regarding Claim 15, John discloses a diode 44 coupled directly between the power supply and the output terminal with no intervening circuits, the diode adapted to mitigate current flow from the power supply to the output terminal (44 is reverse biased from 18 to 22).

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (US 2002/0050615, Ker '615). Regarding Claim 10, John and Ker '109 do not disclose a thyristor device. Ker '615 discloses an ESD protection circuit (see Figure 7b) comprising a clamping device which is a thyristor (see nSCR device). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of John and Ker '109, and to use a thyristor in place of the MOS transistor, because Ker '615 teaches the use of thyristor as ESD clamping device for the protection of integrated circuits from ESD and EOS.

Response to Arguments

9. Applicant's arguments filed on 2/25/2010 have been fully considered.

Regarding Applicant's arguments on Pages 8-9 of the Remarks toward drawing objections, examiner notes that the objection under 37 CFR 1.82(a) is for the **claimed elements** a parasitic npn transistor of Claim 9, and a thyristor of Claim 10, not shown in

the drawings, not for the details not shown as described in the specification (both objections are under37 CFR 1.82(a)).

Regarding Applicant's arguments on Page 9 of the Remarks toward the objection to the specification, examiner notes that the objection is that no explanation of the time delay circuit is given, to provide information on how the time delay circuit affects the circuit operation, when **specific operation of the circuit/s** is discussed. On Page 8-9 of the Specification describes MN1 driving the node NET1 as fast as possible, and the resistor is described as protecting MN1. It is noted the claimed time delay circuit includes resistor and capacitive device, or R and MN1. Examiner further notes that the presence of resistor in fact increase the time constant of the RC circuit formed by MN1 and R, so decreases the speed of response of the time delay circuit.

Regarding Chin reference, the Applicant argues that the reference fails to teach a time delay circuit as recited in Claim 1.

In response, examiner notes that the primary reference Krakauer discloses a time delay circuit formed by transistor 42. Krakauer's time delay circuit has capacitance of 42 and resistance of connection means and that of 42. Krakauer does not specifically disclose a resistor. Chin is relied upon for the teaching of a resistor in series with a diode connected MOS transistor to protect the transistor against high ESD stress voltages (Column 3, lines 38-40). Examiner further notes that instant application also describe the function of the resistor as protecting the MOS transistor MN1 (Specification, see table on Pages 8-9).

Regarding Krakauer reference, the Applicant argues that the capacitive device 42 of Krakauer is not connected to a power supply.

In response, examiner notes that 42 is connected to 16, and 16 is connected to pad 12 which provides a voltage VPAD to 16, when PAD is supplied with a voltage, also notes that 16 is connected to VDD of 14, and provides the VDD voltage to 16 depending on the ON/OFF status of transistors of 14.

Regarding Applicant's arguments that the Krakauer reference teaches away from connecting the transistor 42 to a power supply.

In response, examiner notes that Krakauer does not teaches away from connecting 40 to Vdd, only provides a solution to save space and cost by providing a self-referencing modulation circuit. It is true that in Column 4, lines 59-67, Krakauer discloses that for the embodiment in Figure 2 there is no need to provide a connection between the modulation circuit and any reference voltage supply voltage Vdd, as the circuit is configured to act as a self referencing modulation circuit (a self referencing circuit saves space and cost). Krakauer also discloses the prior art teaching of the connection of modulation circuit to Vdd.

Regarding Applicant arguments toward the voltage applied to the Vpad, examiner notes that Arguments conflicts with Claim 2 of the instant application that limits the pad 2 as a signal pad or power supply voltage, or that the voltage applied to pad 2 is a signal or power supply voltage, and the protection circuit can be used to protect a circuit from ESD applied to an signal pad or power supply pad.

Regarding Applicant's arguments that transistor 42 is not a capacitive device, examiner notes that in Column 4, lines23-26, Krakauer discloses, "modulation circuit 40 includes a high impedance resistor 42, here a diode connected p-type metal-oxide semiconductor (PMOS) device". A diode connected transistor is capacitive as well as resistive, and is high impedance as the diode is not turned on until the threshold voltage is met.

Regarding John reference, the Applicant argues on Page 7 of the Remarks that John reference ('511 reference) expressly teaches that a capacitive device should not be used, referring to John, Column 2, lines 14-17.

Examiner respectfully disagrees. In Column 2, lines 14-17, John discloses, "The ESD detector does not include **capacitors** for sensing of the ESD event thus is not susceptible to false triggering when used in high-speed digital circuitry." It can be seen that John is referring to capacitors not capacitive device, and the diode connected transistor, and diodes of the ESD detector 30 of John are capacitive devices.

Regarding Applicant's arguments toward Avery reference are rendered moot as the reference is withdrawn from the rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yu et al. (US 4,802,054), Tyler et al. (US 2003/0202300).

US 5,717,648 to Davis et al. teaches resistive-capacitive delay of word lines. US 5,581,199 to Pierce et al. teaches resistive-capacitive delay in signal lines.

US 5,717,324 to Tobita teaches diode connected MOS transistor in series with resistor.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy Thomas whose telephone number is 571-272-6002. The examiner can normally be reached on Monday - Friday 8:00 AM - 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fureman Jared can be reached on 571-272-2391. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lucy Thomas/
Examiner, Art Unit 2836, 3/30/2010
/Fritz M Fleming/

Primary Examiner, Art Unit 2836